ABSTRACT OF THE DISCLOSURE

The present invention provides a fundamental cell, semiconductor integrated circuit device, wiring method and wiring apparatus for designing a layout of a functional circuit block or a semiconductor integrated circuit device using the fundamental cells, with a higher degree of freedom of wirings. The connection terminals 2 and 3 of the fundamental cell 1 are terminals for supplying the power source voltage VDD and ground potential VSS to the N and P type wells. The terminals may be defined as a contact structure between a metal layer and N and P type well areas, and alternatively defined as stacked VIA structure for multilayered metal wiring layers and N and P type well areas if desired in correspondence with the manufacturing process used for manufacturing the semiconductor integrated circuit device implementing the fundamental cell 1. The fundamental cell 1 has neither the connection terminals 2 and 3, nor the power source voltage VDD and ground potential VSS to those two PMOS and NMOS transistors.